

Incremental, Assertion-Based Design Verification

ABSTRACT

5 A design verification system includes a first verification engine to model the operation of
a first design of an integrated circuit to obtain verification results including the model's
adherence to a property during N time steps of its operation, proofs that one or more verification
targets can be reached, and verification coverage results for targets that are not reached. A
correspondence engine determines the functional correspondence between the first design and a
10 second design of the integrated circuit. Functional correspondence, if demonstrated, enables
reuse of the first engine's verification results to reduce resources expended during subsequent
analysis of the second design. The correspondence determination may be simplified using a
composite model of the integrated circuit having "implies" logic in lieu of "EXOR" logic. The
implies logic indicates conditions in which a node in the second design achieves a state that is
15 contrary to the verification results for the first design.